have measured oxygen transmission rates (OTR) and water vapor transmission rates (WVTR) values well below the detection limits of current industrial instrumentation used for permeation measurements (Mocon OxTran 2/20L and Permatran). Table 1 shows the OTR and WVTR values (measured according to ASTM F 1927–98 and ASTM 1249–90, respectively) measured at Mocon (Minneapolis, Minn.) for several barrier stacks on 7 mil PET along with reported values for other materials.

TABLE 1

	Oxygen Permeation Rate ($cc/m^2/day$)		Water Vapor Permeation ($g/m^2/day$)+	
Sample	23° C.	38° C.	23° C.	38° C.
Native 7 mil PET	7.62	—	—	—
1-barrier stack	<0.005	<0.005*	—	0.46+
1-barrier stack with ITO	<0.005	<0.005*	—	0.011+
2-barrier stacks	<0.005	<0.005*	—	<0.005+
2-barrier stacks with ITO	<0.005	<0.005*	—	<0.005+
5-barrier stacks	<0.005	<0.005*	—	<0.005+
5-barrier stacks with ITO	<0.005	<0.005*	—	<0.005+
DuPont film[1] (PET/Si_3N_4 or PEN/Si_3N_4)	0.3	—	—	—
Polaroid film[1]	<1.0	—	—	—
PET/Al[2]	0.6	—	0.17	—
PET/silicon oxide[2]	0.7–1.5	—	0.15–0.9	—
Teijin LCD film (HA grade - TN/STN)[3]	<2	—	<5	—

*38° C., 90% RH, 100% O_2
+38° C. 100% RH
1-P.F. Carcia, 46th International Symposium of the American Vacuum Society, Oct. 1999
2-Langowski, H.C., 39th Annual Technical Conference Proceedings, SVC, pp. 398–401 (1996)
3-Technical Data Sheets

As the data in Table 1 shows, the barrier stacks of the present invention provide oxygen and water vapor permeation rates several orders of magnitude better than PET coated with aluminum, silicon oxide, or aluminum oxide. The barrier stacks are extremely effective in preventing oxygen and water penetration to the underlying components, substantially outperforming other barrier coatings on the market. The barrier stacks have an oxygen transmission rate of less than 0.005 $cc/m^2/day$ at 23° C. and 0% relative humidity, an oxygen transmission rate of less than 0.005 $cc/m^2/day$ at 38° C. and 90% relative humidity, and a water vapor transmission rate of less than 0.005 $g/m^2/day$ at 38° C. and 100% relative humidity. The actual transmission rates of the barrier stacks is less than this, but it cannot be measured with existing equipment.

Semiconductor passivation is compatible with flexible and rigid semiconductor substrates. The barrier stacks can be deposited in a batch, in-line or cluster tool, or on thin film transistors deposited on flexible substrates, such as metal foils and polymeric webs. The encapsulation/barrier stack deposition process is compatible with integrated circuit fabrication processes and does not damage sensitive microcircuitry and active devices. The barrier stacks can be deposited over nonuniform surfaces and can effectively encapsulate and planarize surface features.

Because the preferred process involves flash evaporation of a monomer and magnetron sputtering, deposition temperatures are below 100° C., which is much less than the 300° C. to 800° C. temperatures required for CVD coating processes, and stresses in the coating can be minimized. Because of the low temperatures, the process does not harm or degrade temperature sensitive components. Multilayer coatings can be deposited at high deposition rates. No harsh gases or chemicals are used, and the process can be scaled up to large substrates and wide webs. The barrier properties of the coating can be tailored to the application by controlling the number of layers, the materials, and the layer design.

The encapsulation process of the present invention provides improved encapsulation of microelectronic devices on semiconductor substrates. In addition to the improved barrier properties, the chemical resistance, thermal and shock resistance, mechanical robustness, and coating quality are also improved. As a result, the lifetime of the encapsulated microelectronic devices is significantly increased.

Thus, the present invention provides a barrier stack with the exceptional barrier and other properties necessary for hermetic sealing of an microelectronic device.

While certain representative embodiments and details have been shown for purposes of illustrating the invention, it will be apparent to those skilled in the art that various changes in the compositions and methods disclosed herein may be made without departing from the scope of the invention, which is defined in the appended claims.

What is claimed is:

1. An encapsulated microelectronic device comprising:

a semiconductor substrate;

a microelectronic device adjacent to the semiconductor substrate, the microelectronic device being selected from integrated circuits, charge coupled devices, metal sensor pads, micro-disk lasers, electrochromic devices, photochromic devices, microelectromechanical systems and solar cells; and

at least one first barrier stack comprising at least one first barrier layer and at least one first polymer layer, the at least one first barrier stack adjacent to the microelectronic device on a side opposite the semiconductor substrate, wherein the at least one first barrier stack encapsulates the microelectronic device.

2. The encapsulated microelectronic device of claim **1** further comprising at least one second barrier stack located between the semiconductor substrate and the microelectronic device, the at least one second barrier stack comprising at least one second barrier layer and at least one second polymer layer.

3. The encapsulated microelectronic device of claim **1** wherein the at least one first barrier layer is substantially transparent.

4. The encapsulated microelectronic device of claim **2** wherein the at least one second barrier layer is substantially transparent.

5. The encapsulated microelectronic device of claim **1** wherein at least one of the at least one first barrier layers comprises a material selected from metal oxides, metal nitrides, metal carbides, metal oxynitrides, metal oxyborides, and combinations thereof.

6. The encapsulated microelectronic device of claim **5** wherein the metal oxides are selected from silicon oxide, aluminum oxide, titanium oxide, indium oxide, tin oxide, indium tin oxide, tantalum oxide, zirconium oxide, niobium oxide, and combinations thereof.

7. The encapsulated microelectronic device of claim **5** wherein the metal nitrides are selected from aluminum nitride, silicon nitride, boron nitride, and combinations thereof.

8. The encapsulated microelectronic device of claim **5** wherein the metal oxynitrides are selected from aluminum oxynitride, silicon oxynitride, boron oxynitride, and combinations thereof.